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OIPE JUL 31 2002 PATENT & TRADEMARK OFFICE

EXPEDITED PROCEDURE - EXAMINING GROUP 2123

S/N 09/031,326 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Joseph J. Karniewicz	Examiner: Thai Phan	
Serial No.:	09/031,326	Group Art Unit: 2123	
Filed:	February 26, 1998	Docket: 303.376US1	
Title:	PARAMETER POPULATION OF CELLS OF A HIERARCHICAL SEMICONDUCTOR STRUCTURE VIA FILE RELATION		

RECEIVED AUG 0 8 2002 Technology Center 2100

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AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

Box RCE
Commissioner for Patents
Washington, D.C. 20231

In response to the Final Office Action mailed February 26, 2002, please amend the application as follows:

This response is accompanied by a Petition, as well as the appropriate fee, to obtain a two-month extension of the period for responding to the Office action, thereby moving the deadline for response from May 26, 2002 to July 26, 2002.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 1, 9, 15, and 22. The specific amendments to individual claims are detailed in the following marked up set of claims.

1. (Amended) A system for populating parameters of design cells defining the physical layout of a hierarchical semiconductor structure comprising:

a global file of global geometric variables relating to a physical layout of element blocks of the hierarchical semiconductor structure;

a plurality of local files, each local file containing parameters relating a plurality of local variables to the global geometric variables; and,

a plurality of programmable design cells, each cell corresponding to a local file and having a set of parameters created by relating the corresponding local variables within a local file